

# Setareh Behroozi

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## EDUCATION

### University of Wisconsin–Madison

Ph.D. Student, Electrical and Computer Engineering Jan 2017 – Present

Advisor: Professor Younghyun Kim

### Sharif University of Technology, Tehran, Iran

M.S., Computer Engineering Sep 2013 – Aug 2015

Advisor: Professor Hamid Sarbazi-Azad

### Iran University of Science and Technology, Tehran, Iran

B.S., Computer Engineering Sep 2009 – Aug 2013

Advisor: Professor Mahmood Fathy

## RESEARCH INTERESTS

Low-power design

Computer architecture

Approximate computing

Internet-of-Things

Embedded systems

Emerging technologies

## AWARDS & HONORS

**Foxconn “Smart Cities-Smart Futures” Competition Final Winner**, for “SmartID” project 2019

**Foxconn “Smart Cities-Smart Futures” Competition Final Winner**, for “Nightshift” project 2019

**CRA-W Grad Cohort for Women Workshop Student Scholarship** 2019

**Electrical and Computer Engineering Chancellor’s Opportunity Fellowship (COF)** 2018

**ISLPED Low-Power Design Contest Award**, International Symposium on Low Power Electronics and Design (ISLPED) 2018

for “AxSerBus: A Quality-Configurable Approximate Serial Bus for Energy-Efficient Sensing”

**Grace Hopper Celebration (GHC) Student Scholarship** 2018

**A. Richard Newton Young Student Fellowship**, Design Automation Conference (DAC) 2017

**SIGDA University Demo Finalist**, Design Automation Conference (DAC) 2017

for “AxSerBus: Approximate Serial Bus for Energy-Efficient Sensing”

**Master’s Degree Admission Examination**, Ranked 23 in the field of Computer Engineering among 32276 participants 2013

**Iran Game Development Cup (Iran GDC)**, Second place, Kashan, Iran 2012

**Best Game Design Award**, Iran Game Development Cup (Iran GDC), Kashan, Iran 2012

**Virtual Robot Competition**, Third place, Iran Open Robotic Competition, Tehran, Iran 2010

## PUBLICATIONS

### JOURNAL


[2] Jackson Melchert, **Setareh Behroozi**, Jingjie Li, and Younghyun Kim, “SAADI-EC: A Quality-Configurable Approximate Divider for Energy Efficiency,” *IEEE Transaction on VLSI Systems (TVLSI)*, vol. 27, no. 11, pp. 2680-2692, 2019

[1] **Setareh Behroozi**, Vijay Raghunathan, Anand Raghunathan, and Younghyun Kim, “A Quality-Configurable Approximate Serial Bus for Energy-Efficient Sensory Data Transfer,” *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, vol. 8, no. 3, pp. 379–390, 2018

### CONFERENCES

[4] Younghyun Kim, Joshua San Miguel, **Setareh Behroozi**, Tianen Chen, Kyuin Lee, Yongwoo Lee, Jingjie Li, and Di Wu, “Approximate Hardware Techniques for Energy-Quality Scaling Across the System,” *International Conference on Electronics, Information, and Communication (ICEIC)*, Barcelona, Spain, 2020

[3] **Setareh Behroozi**, Jingjie Li, Jackson Melchert, and Younghyun Kim, “SAADI: A scalable accuracy approximate divider for dynamic energy-quality scaling”, *Asia South Pacific Design Automation Conference (ASP-DAC)*, pp. 481–486, Tokyo, Japan, 2019

- [2]  Younghyun Kim, **Setareh Behroozi**, Vijay Raghunathan, and Anand Raghunathan, “AxSerBus: A Quality-Configurable Approximate Serial Bus for Energy-Efficient Sensing,” in *Proceedings of International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 1–6, Taipei, Taiwan, 2017  
[Low-Power Design Contest Award at ISLPED 2018](#)
- [1] **Setareh Behroozi** and Iraklis Anagnostopoulos, “Application Resource Management for Exploitation of NVM in Distributed Shared Memory Systems,” in *Proceedings of International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, Baltimore, Maryland, 2017

<b>PRESENTATIONS</b>	<b>CRA-W Grad Cohort for Women Workshop (poster)</b>	Apr 2019
	CRA-W Grad Cohort for Women Workshop Energy-Quality Scalable Systems	
	<b>Computer Architecture Affiliates Meeting</b>	Oct 2018
	University of Wisconsin–Madison Parrot: A Decoupled Architecture for Non-Volatile Caches	
	<b>ISLPED Low-Power Design Contest (poster)</b>	Jul 2018
	International Symposium on Low Power Electronics and Design (ISLPED) AxSerBus: A Quality-Configurable Approximate Serial Bus for Energy-Efficient Sensing	
	<b>Computer Architecture Affiliates Meeting</b>	Oct 2017
University of Wisconsin–Madison AxSerBus: A Quality-Configurable Approximate Serial Bus for Energy-Efficient Sensing		
	<b>SIGDA University Demo (poster)</b>	Jun 2017
Design Automation Conference (DAC) AxSerBus: A Quality-Configurable Approximate Serial Bus for Energy-Efficient Sensing		
	<b>A. Richard Newton Young Student (poster)</b>	Jun 2017
Design Automation Conference (DAC) AxSerBus: A Quality-Configurable Approximate Serial Bus for Energy-Efficient Sensing Application Resource Management for Exploitation of NVM in Distributed Shared Memory Systems		

<b>RESEARCH EXPERIENCE</b>	<b>DOCTORAL RESEARCH ASSISTANT</b>	Jan 2017 – Present
	Wisconsin Embedded System and Computing (WISEST) Laboratory University of Wisconsin–Madison, Madison, WI	

Major projects:

**Energy-efficient computing**, developing approximate architectures and system-level techniques for improving the energy efficiency of mobile, wearable Internet-of-Things, and implantable medical devices.

- Approximate non-linear operations via Taylor series: Implementing a quality scalable unified nonlinear processing element for emerging neural network models.
- Approximate non-volatile cache: Performing research on emerging memory technologies, focusing on non-volatile memories in last-level cache architecture for improving the energy consumption and endurance of the system.
- SAADI: Implementing a quality scalable low-power divider unit for energy efficient signal processing (presented at ASP-DAC 2019 and TVLSI 2019).

- AxSerBus: Designing a configurable approximate serial bus encoding for energy-efficient data transfer in off-chip interconnects as well as performing research on full system approximation control scheme for optimizing the energy-efficiency and application quality (presented at ISLPED 2017 and JETCAS 2018).
- MyoAuth: Developed a biometric user-authentication system using dynamic electromyography in keystroke transition for enhancing the security of password-based authentication schemes without using energy-hungry security augmentation techniques (ECE 901).
- PIM: Developed a processing in memory (PIM) architecture using ReRAM crossbar for energy efficient convolution operation (ECE 756).
- WISC processor: Implemented a fully pipelined processor in synthesizable Verilog (ECE 552).

#### DOCTORAL RESEARCH ASSISTANT

Aug 2015 – Dec 2016

Embedded System Software Laboratory  
Southern Illinois University, Carbondale, IL

Major projects:

**Energy-efficient multi and many-core systems**, performed research on system-level and architecture-level techniques on many-core systems to improve the energy consumption of the system exploiting emerging technologies.

- Application research management: Developed an application mapping scheme for many-core platforms with non-volatile memory architecture to decrease the power consumption and improve the system lifetime (presented at ISCAS 2017).
- Near-optimal application mapping: Designed an optimized application mapping using the genetic algorithm for many-core systems with multiple constraints such as power consumption, temperature, and memory endurance (CS 591).

**VLSI testing**, performed research on design automation in VLSI circuit testing to reduce the required test time.

- Implemented a test pattern generation algorithm for VLSI circuit testing based on PODEM algorithm (ECE 522).

#### GRADUATE RESEARCH ASSISTANT

Sep 2013 – Aug 2015

High-Performance Computing Architecture and Networks (HPCAN) Laboratory  
Sharif University of Technology, Tehran, Iran Major projects:

**Low-power and high-performance computing**, performed research on system-level, architecture-level, and circuit-level techniques to improve the energy consumption of the system.

- Non-volatile last level cache: Introduced an architecture-level technique for non-volatile last level cache for prolonging the lifetime of the system (M.S. thesis).
- Low-power FPGA: Developed a tree-based algorithm for improving the energy efficiency of the FPGA architecture synthesized by VPR and ABS tools (CE 648).
- Cache simulator: Implemented a cache simulator including state-of-the-art replacement and prefetching policies (CE 723).
- Low-power arithmetic units: Implemented a low-power array multiplier using dual voltage threshold technique (CE 727)

**UNDERGRADUATE RESEARCH ASSISTANT** Sep 2012 – Sep 2013  
High-Performance Computing Laboratory  
Iran University of Science of Technology, Tehran, Iran

Major projects:

**Reconfigurable cache**, designed a reconfigurable cache to perform high-speed computational operations to improve the performance of the system (B.S. thesis)

**UNDERGRADUATE RESEARCH ASSISTANT** Sep 2010 – Aug 2013  
Game Development and Research Laboratory  
Iran University of Science of Technology, Tehran, Iran

Major projects:

**IUST game engine**, implemented an open-source 3D game engine under Linux platform, using Ogre3D, Qt and Nvidia PhysX for physic simulation.

**Game texture and materials**, designed texture and materials in 3D games for independent and educational games.

## TEACHING EXPERIENCE

### INSTRUCTOR

- ENG 222, **Computational Methods for Engineers and Technologists** Fall 2016  
Southern Illinois University, Carbondale, IL.
- ECE 222, **Intro to Digital Computation** Spring 2016  
Southern Illinois University, Carbondale, IL.
- CE 40401, **Industrial Automation Laboratory** Fall 2014  
Sharif University of Technology, Tehran, Iran.

### TEACHING ASSISTANT

- CS 537, **Introduction to Operating Systems** Spring 2019  
University of Wisconsin–Madison, Madison, WI (~280 students).
- ECE 551, **Digital System Design and Synthesis** Spring 2018  
University of Wisconsin–Madison, Madison, WI.
- CE 409123, **Computer Fundamentals and Programming** Fall 2010  
Iran University of Science and Technology, Tehran, Iran.

## SERVICES

### EXTERNAL REVIEWER

Transaction on Computers 2020  
Design Automation Conference (DAC) 2018, 2019 , 2020  
International Symposium on Low Power Electronics and Design (ISLPED) 2017, 2018, 2019  
Asia and South Pacific Design Automation Conference (ASP-DAC) 2018, 2019  
International Conference on VLSI Design (VLSID) 2019  
IEEE Transactions on Circuits and Systems II 2019  
Symposium on Applied Computing (SAC) 2018

### VOLUNTEER SERVICES

Graduate Student Association (GSA) member Aug 2017 – Present  
Department of Electrical and Computer Engineering representative in the College of Engineering (CoE) Graduate Student Advisory Committee Aug 2017 – May 2019

**RELATED COURSES**

Embedded computing systems	Reconfigurable computing
Low power design	VLSI circuit testing
Advanced computer architecture	Interconnection networks
Advanced topics on ASIC design	Digital VLSI design
Hardware security and encryption	Machine learning
Design automation of digital systems	Data mining

**SKILLS**

**Programming language:** C, C++, Python, Java, Bash, Verilog, VHDL

**CAD tools and simulators:** MATLAB, Gem5, Sniper, CACTI, NVSIM, VTR, Hspice, Cadence, Tetramax, Synopsys Design Compiler, ModelSim.